IN THE CLAIMS

Please enter the below clarifying claim amendments.

1. (currently amended) An apparatus, comprising:

a transaction queue to store pending device transactions and dispatched device transactions, the queue including an input for receiving transactions, the queue including an output for dispatching transactions to a device, the device transactions including device read transactions and device write transactions; and

a controller coupled to the transaction queue and responsive to an invalid data signal for a device read transaction to prevent the transaction queue from dispatching a pending transaction to the device, to cause the transaction queue to dispatch again the device read transaction which resulted in the invalid data signal **such that a memory location is accessed more than once to obtain valid data** and, subsequently, to send to a desired destination a data available signal for the data which resulted from the device read transaction which was dispatched again, and to enable the transaction queue to dispatch a pending transaction to the device.

2. (original) The apparatus of claim 1 wherein the controller is further responsive to the invalid data signal to determine if invalid data read from the device location has occurred previously and, if not, to then cause the transaction queue to dispatch again the device read transaction which resulted in the invalid data signal and, subsequently, to send to a desired destination a data available signal for the data which resulted from the device read transaction which was dispatched again, and to enable the transaction queue to dispatch a pending transaction to the device.

3. (original) The apparatus of claim 1 wherein the controller is further responsive to the invalid data signal to determine if invalid data read from the device location has occurred previously and, if so, then to send to the desired destination a data available signal for the data which resulted from the device read transaction which resulted in the invalid data signal.

4. (original) The apparatus of claim 1 and wherein the controller is further responsive to the invalid data signal to cause intervening data to be cleared, intervening data being data which was read from device locations other than that device location which produced the invalid data and which was read between the time data was read from that device location and the time data was read again from that device location, and then, after causing the data which was read again from the device to be sent to the desired destination, to cause the data to be read again from device

locations which were read between the time data was read from that device location and the time data was read again from that device location and, subsequently, to send to the desired destination a data available signal for the data which was read again from those device locations.

5. (original) The apparatus of claim 1 and wherein the transaction queue further includes first pointer for pending transactions and a second pointer for dispatched transactions, and the controller is further responsive to the invalid data signal to cause the second pointer to assume the value of the first pointer.

6. (original) The apparatus of claim 1 wherein invalid data is data which has an uncorrectable error.

7. (currently amended) An apparatus, comprising:

a memory device to read and write data in response to device transactions, the device transactions including device read transactions and device write transactions;

a data utilization device to accept data in response to a data available signal;

a memory controller, coupled to the memory device and to the data utilization device, to accept data from the memory device, to check the data for an error, to provide an invalid data signal if the data has an error, and to provide the data from the memory to the data utilization device;

a transaction queue, coupled to the memory controller, to store pending device transactions and dispatched device transactions, the queue including an input for receiving transactions, the queue including an output for dispatching transactions to the memory controller; and

a master controller, coupled to the memory controller, the transaction queue and the data utilization device, and responsive to an invalid data signal for a device read transaction to prevent the transaction queue from dispatching a pending transaction to the memory controller, to cause the transaction queue to dispatch again the device read transaction which resulted in the invalid data signal **such that a memory location is accessed more than once to obtain valid data** and, subsequently, to send to the data utilization device a data available signal for the data which resulted from the device read transaction which was dispatched again, and to enable the transaction queue to dispatch a pending transaction to the memory controller.

8. (original) The apparatus of claim 7 wherein the master controller is further responsive to the invalid data signal to determine if invalid data read from the device location has occurred

previously and, if not, to then cause the transaction queue to dispatch again the device read transaction which resulted in the invalid data signal and, subsequently, to send to the data utilization device a data available signal for the data which resulted from the device read transaction which was dispatched again, and to enable the transaction queue to dispatch a pending transaction to the memory controller.

9. (original) The apparatus of claim 7 wherein the master controller is further responsive to the invalid data signal to determine if invalid data read from the device location has occurred previously and, if so, then to send to the data utilization device a data available signal for the data which resulted from the device read transaction which resulted in the invalid data signal.

10. (original) The apparatus of claim 7 and wherein the master controller is further responsive to the invalid data signal to cause intervening data to be cleared, intervening data being data which was read from device locations other than that device location which produced the invalid data and which was read between the time data was read from that device location and the time data was read again from that device location, and then, after sending to the data utilization device a data available signal for the data which was read again from that device location, to cause the data to be read again from device locations which were read between the time data was read from that device location and the time data was read again from that device location and, subsequently, to send to the data utilization device a data available signal for the data which was read again from those device locations.

11. (original) The apparatus of claim 7 and wherein the transaction queue further includes first pointer for pending transactions and a second pointer for dispatched transactions, and the master controller is further responsive to the invalid data signal to cause the second pointer to assume the value of the first pointer.

12. (original) The apparatus of claim 7 wherein the memory controller, after checking the data for an error, is further operative to attempt to correct the invalid data and, if the invalid data cannot be corrected, then to send the invalid data signal.

13. (currently amended) A method, comprising:

receiving an indication that data read from a device location is not valid;

inhibiting write operations to the device;

reading the data from that device location again **such that the data in the device location is accessed more than once to obtain valid data**; and

enabling write operations to the device and sending to a desired destination a valid data signal for the data which resulted from reading that device location again.

14. (original) The method of claim 13 and, prior to inhibiting write operations,

if invalid data from that device location has not occurred previously then proceeding with inhibiting write operations, reading the data again, enabling write operations and sending the valid data signal.

15. (original) The method of claim 13 and:

if invalid data read from that device location has not occurred previously then setting a previous error flag to indicate that invalid data from that device location has occurred previously; and

if invalid data read from that device location has occurred previously then clearing the previous error flag to indicate that invalid data from that device location has not occurred previously.

16. (original) The method of claim 13 in which invalid data is data which has an uncorrectable error.

17. (currently amended) A method, comprising:

receiving an indication that data read from a device location is invalid;

if invalid data read from the device location has occurred previously then sending a valid data signal for the data to a desired destination; and

if invalid data read from the device location has not occurred previously then:

inhibiting write operations to the device;

reading the data in that device location again **such that the data in the device location is accessed more than once to obtain valid data**; and

enabling write operations to the device and sending to a desired destination a valid data signal for the data which resulted from reading that device location again.

18. (original) The method of claim 17 and, prior to inhibiting write operations,

if invalid data from that device location has not occurred previously then proceeding with inhibiting write operations, reading the data again, enabling write operations and sending the valid data signal.

19. (original) The method of claim 17 and:

if invalid data read from the device location has not occurred previously then setting a previous error flag to indicate that invalid data read from that device location has occurred previously; and

if invalid data read from the device location has occurred previously then clearing the previous error flag to indicate that invalid data read from that device location has not occurred previously.

20. (original) The method of claim 17 in which invalid data is data which has an uncorrectable error.